In the Claims:

Claim 1 (currently amended): An integrated circuit chip formed in a semiconductor substrate, comprising:

a first interconnect metal layer in said semiconductor substrate;

a first intermetallic dielectric layer in said semiconductor substrate situated over said first interconnect metal layer;

a metal resistor in said semiconductor substrate situated over said first intermetallic dielectric layer, said metal resistor being only connected to a second interconnect metal layer;

a dielectric cap layer in said semiconductor substrate patterned on said metal resistor;

a second intermetallic dielectric layer in said semiconductor substrate formed over said dielectric cap layer and said metal resistor;

said second interconnect metal layer in said semiconductor substrate being situated over said second intermetallic dielectric layer~~, wherein said first and second interconnect metal layers are adjacent to each other~~;

a first intermediate via in said semiconductor substrate connected to a first terminal of said metal resistor, said first intermediate via being further connected to a first metal segment patterned in said second interconnect metal layer;

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a second intermediate via in said semiconductor substrate connected to a second terminal of said metal resistor, said second intermediate via being further connected to a second metal segment patterned in said second interconnect metal layer.

Claim 2 (original): The integrated circuit chip of claim 1 wherein said metal resistor is selected from the group consisting of titanium nitride and tantalum nitride.

Claim 3 (original): The integrated circuit chip of claim 1 wherein said first interconnect metal layer comprises aluminum.

Claim 4 (original): The integrated circuit chip of claim 1 wherein said first intermetallic dielectric layer comprises HDPCVD silicon dioxide.

Claim 5 (original): The integrated circuit chip of claim 1 wherein said second intermetallic dielectric layer comprises undoped silica glass.

Claim 6 (canceled).

Claim 7 (previously presented): The integrated circuit chip of claim 1 wherein said dielectric cap layer comprises silicon nitride.

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Claim 8 (original): The integrated circuit chip of claim 1 further comprising an oxide cap layer situated between said metal resistor and said first intermetallic dielectric layer.

Claim 9 (original): The integrated circuit chip of claim 8 wherein said oxide cap layer comprises PECVD silicon dioxide.

Claim 10 (currently amended): An integrated circuit chip formed in a semiconductor substrate, comprising:

a first interconnect metal layer in said semiconductor substrate;

a first intermetallic dielectric layer in said semiconductor substrate situated over said first interconnect metal layer;

a metal resistor in said semiconductor substrate situated over said first intermetallic dielectric layer, said metal resistor being only connected to a second interconnect metal layer;

a dielectric cap layer in said semiconductor substrate patterned on said metal resistor;

a second intermetallic dielectric layer in said semiconductor substrate formed over said dielectric cap layer and said metal resistor;

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said second interconnect metal layer in said semiconductor substrate being situated over said second intermetallic dielectric layer~~, wherein said first and second interconnect metal layers are adjacent to each other~~;

a first intermediate via in said semiconductor substrate connected to a first terminal of said metal resistor and said second interconnect metal layer;

a second intermediate via in said semiconductor substrate connected to a second terminal of said metal resistor and said second interconnect metal layer.

Claim 11 (original): The integrated circuit chip of claim 10 wherein said metal resistor is selected from the group consisting of titanium nitride and tantalum nitride.

Claim 12 (original): The integrated circuit chip of claim 10 wherein said first intermetallic dielectric layer comprises HDPCVD silicon dioxide.

Claim 13 (original): The integrated circuit chip of claim 10 wherein said second intermetallic dielectric layer comprises undoped silica glass.

Claim 14 (canceled).

Claim 15 (previously presented): The integrated circuit chip of claim 10 wherein said dielectric cap layer comprises silicon nitride.

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Claim 16 (original): The integrated circuit chip of claim 10 wherein said first interconnect metal layer comprises aluminum.

Claim 17 (original): The integrated circuit chip of claim 10 further comprising an oxide cap layer situated between said metal resistor and said first intermetallic dielectric layer.

Claim 18 (original): The integrated circuit chip of claim 17 wherein said oxide cap layer comprises PECVD silicon dioxide.

Claims 19-27 (canceled).

Claim 28 (previously presented): The integrated circuit chip of claim 1 wherein said metal resistor is not connected from below.

Claim 29 (previously presented): The integrated circuit chip of claim 1 wherein the thickness of said metal resistor is approximately 100.0 Angstroms to 1500.0 Angstroms.

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Claim 30 (previously presented): The integrated circuit chip of claim 10 wherein said metal resistor is not connected from below.

Claim 31 (previously presented): The integrated circuit chip of claim 10 wherein the thickness of said metal resistor is approximately 100.0 Angstroms to 1500.0 Angstroms.

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